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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/743,113	12/22/2003	Kyung Yun Jung	SUN-DA-114T	8491

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EXAMINER

MONDT, JOHANNES P

ART UNIT	PAPER NUMBER
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3663

DATE MAILED: 12/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/743,113

Applicant(s)

JUNG, KYUNG YUN

Examiner

Johannes P. Mondt

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 29 September 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-3 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/02/06 has been entered.

### ***Response to Amendment***

Amendment After Final Rejection, filed 9/29/06, has been entered, following said RCE. In said Amendment Applicant substantially amended claims 1-3 through substantial amendment of claims 1 and 3. Comments submitted in Remarks submitted with said Amendment are included below under "Response to Arguments".

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. ***Claims 1-3*** are rejected under 35 U.S.C. 102(e) as being unpatentable over Lehmann et al (US 2004/0217441 A1) (previously cited) in view of Lee (5,208,177), and , in an alternative rejection, in view of Lee (loc.cit.) and Ghandi et al (6,448,631 B2).

*Lehmann et al teach* (Figure 11; [0109]-[0117]) a semiconductor device ([0054]) comprising:

a capacitor having a bottom electrode (source/drain regions 143, 146, 143a, 146a) ([0106] with channel in substrate between 143 and 146 therebetween),

a dielectric layer 124, 124a, 124b (anti-fuse layer is a dielectric: see [0004], [0080]; cf. [0106]) formed on the bottom electrode (Figure 11), the capacitor being formed on a semiconductor substrate 101 (Figure 11 and [0054]) and an upper electrode 125, 125a, 125b ([0080] and [0106]) formed on said dielectric layer ([0054]), wherein the bottom electrode, dielectric layer and upper electrode are vertically arranged (Figure 11);

a first insulating layer 103 ([0110] and [0054]) formed on the semiconductor substrate 101 ([0110] and [0054]) to cover the capacitor (Figure 11): said first insulating layer can either be defined as the layer portion of 103 with a lateral extent confined to the area of the device components as recited, i.e., the portion underneath 123 in Figure 10, or, in the alternative rejection, as the entire layer 103;

a first plurality of first contact plugs 141 and 144 ([0110] and [0074]) electrically connected to the bottom electrode (141 connected to 143, 144 to 146, 141a to 143a, and 144a to 146a, respectively) (Fig. 11) and a second plurality of first contact plugs (the portions in first insulating layer 103 of ground lines G electrically connected to upper electrodes 125, 125a,.. ([0121] and hence necessarily are at least in part in said first insulating layer because said upper electrodes 125 are in said first insulation layer)

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of first contact plugs, wherein the first contact plugs belonging to the first plurality are electrically connected to the bottom electrode or upper electrode;

a first metal wiring 105 ([0054] and [0110]) (Figure 4) formed on the first insulating layer (Figure 11) and connected to the upper electrode through the first contact plugs of the first plurality (namely: through 141 and 144);

a second insulating layer 107 ([0110] and [0054]; Figure 11) formed on the first insulating layer 103;

a second contact plug 127 ([0110] and [0054]) formed on the first insulating layer and connected to the upper electrode 125, 125a,...) through the first contact plugs of the second plurality of first contact plugs, namely the portions of G (loc.cit.);

an anti-fuse 126 ([0110] and [0054]) formed in a certain thickness (an anti-fuse without thickness is impossible because thickness is required in the dielectric phase) in a second via hole (the via hole filled with 161; Fig. 11) of the second insulating layer and electrically connected to the second contact plug (through 161; Figure 11);

a third contact plug 161 ([0110] and [0054]) filling the second via hole on the anti-fuse; and

a second metal wiring (vertical portions of G abutting the upper main surface of said second insulation layer 107; Figure 11) formed on the second insulating layer and electrically connected to the third contact plug (through 127).

*Lehmann et al do not necessarily teach* the limitation that “the third contact plug is formed within the anti-fuse wherein the third contact plug does not directly contact the second insulating layer”.

*However, it would have been obvious to include said limitation in view of Lee,* who, in a patent on improvements of the programmability of anti-fuse devices (title, abstract and "Field of the Invention"), hence analogous art, teaches the anti-fuse dielectric material to be a conformal outer lining 41 around the upper conductive portion of the anti-fuse 42 (see col. 3, l. 10-20) so as to have sharp edges where the electric field is locally enhanced, resulting in a lower value of the required voltage for anti-fuse action (col. 3, l. 21-30) (Figures 4A and 4B). *Motivation* to include the teaching by Lee in the invention by Lehmann immediately derives from the advantage of not having to apply potentially damaging voltages for anti-fuse action (col. 1, l. 35-50) in addition to obvious cost savings due to lower power requirements. *Combination* of said teaching with said invention leads to meeting said limitation with 42 and 41 being the third contact plug and the anti-fuse material (161 and 126, respectively).

This concludes the rejection over Lehmann et al and Lee based on the definition of the first insulating layer as the portion of 103 underneath 123.

In the alternative interpretation of the first insulating layer as the entire insulating layer 103 beyond the boundaries of the device with elements as claimed, neither Lehmann et al nor Lee necessarily teach the limitation that first metal wiring 105 is "on the first insulating layer" 103.

However, it would have been obvious to include said further limitation in view of Ghandi et al, who, in a patent on local interconnect architecture for capacitor structures (N.B.: source/drain – gate structure 404/406/408 is inherently a capacitor structure) (title, abstract, "Field of the Invention"), hence analogous art, teach the fabrication of

metallization lines through deposition on subsequent insulating layers followed by patterning (col. 3, l. 8-47 and Figures 4A and 4B), thus designing each metallization layer to be on the previously deposited insulating layer (Figures 4A and 4B). The limitation is thus seen to be met by conventional cell architecture for local interconnects pertinent to the problem of arranging for local interconnects for capacitor structures, and has the advantage of removing the need for an etching step in the making of said metallization layers. Said advantage is one of time and cost savings in addition to improved integrity of the underlying insulating layers, providing ample motivation to include the teaching by Ghandi et al in the device by Lehmann et al.

On claim 2: second metal wiring as defined above (vertical portion of G abutting upper main surface of 107 as defined above in the discussion of claim 1) is perpendicular to the first metal wiring 105 (see Figure 11).

*On claim 3:* The device of claim 1 would necessarily have to be formed in order to function. Claim 3 fails to further limit the device of claim 1 other than simply form each of their components.

### ***Response to Arguments***

Applicant's arguments filed 9/29/06 have been fully considered but they are not persuasive. In particular, counter to Applicant's argument in traverse on page 4 (Remarks) that "the source/drain regions 143 and 146, dielectric layer 124 and gate electrode 125 of Lehmann et al are not vertically arranged as specified in claims 1 and 3", and that "specific limitations describing the capacitor do not read on a field effect transistor", a MOS capacitor between source/drain regions and gate, with gate

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insulating layer in between is (a) "vertically arranged" both in the OFF state, wherein the channel between source and drain is insulating, and manifestly so in the ON state, wherein said channel is conductive and is part of the capacitor, connecting source and drain vertically underneath the gate and dielectric, said dielectric sandwiched between said gate and said conductive channel. The "vertical arrangement" of said MOS capacitor is generic to the field effect transistor in the ON state while the presence of a third terminal (i.e., a difference in potential between source and drain, does not detract from the inclusion of a capacitor in the field effect transistor, i.e., the MOS Capacitor: see, for instance, S. Wolf, *Silicon Processing for the VLSI Era*", Volume 3, Chapter 3, MOS transistor device physics: Part 1, Basics MOS Physics and the MOS Capacitor, especially pages 83-89, wherein it is made clear that a capacitor (MOS capacitor) is part of the structure of the MOS field effect transistor. That a more complicated dynamics results when the voltages of source and drain are made to differ does not detract from the inclusion of the MOS capacitor in the MOSFET. This is especially relevant for the device invention of Applicant, because a selection of a particular source-drain voltage difference pertains to intended use without impacting the structure. Intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. *In re Casey*, 152 USPQ 235 (CCPA 1967); *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).



In light of the above considerations the arguments in traverse and the amendment do not persuade.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JPM  
November 27, 2006

Patent Examiner:



Johannes Mondt (Art Unit: 3663)